

Dell Controlled Print

Reliability Qualification Requirements for Lead-Free Products

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Engineers/Owners: Dell Reliability Organization

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1.0 Revision History

Revision	ECO	Description	Approved	Date
A00	155640	Initial Release to A00-00	Ed Tinsley	12/17/03
A01	161025	Clarified Reliability scope for process related requirements. Outlined failure modes. Solderability requirements removed. Requirement for component tables removed. Added Sn whisker table. Clarified component delamination criteria per J-STD-020B. Clarified HALT requirement. Reduced the requirements for preconditioning and assembly. Removed ImAg migration testing..	Ed Tinsley	4/28/04

2.0 Introduction

2.1 Purpose/Objective

This document details Dell Corporation's requirements for qualification of lead-free printed circuit board assemblies (PCBAs) supplied directly or indirectly to Dell for use in Dell branded products. These requirements are subject to change based on further industry study and technological changes relating to lead-free solders and parts.

This qualification requirements document is to be used in conjunction with Dell P/N D4394 General Specification for Allowable Levels of Lead (Pb) in Dell Products and Dell P/N M4461 which provides Pb-free requirements for individual components used in Dell products.

2.2 Scope

The requirements listed in this document cover lead-free alloys such as SnCu, SnAg or SnAgCu, with liquidus temperatures below 227°C. Exemptions to Pb-free solder are allowed in Dell products according to the latest RoHS directives (or as determined by Dell's Environmental group). The Dell preferred Pb-free alloy is SnAgCu in the composition range Sn(3.0-4.0)Ag(0.5-0.9)Cu. Lead-free solder alloys with melting temperature greater than 227°C or those containing Bi, In, or Zn are unacceptable at this time due to reliability, supply, and or corrosion concerns. Preferred component lead finish is matte Sn over 1.3µm Ni, however others are acceptable if Sn whisker risk is mitigated. Preferred board finish is immersion Ag (0.15 - 0.5 µm thick). However other surface finishes will also be acceptable in certain applications (i.e. Ni/Au plated, high temperature rated OSP materials, immersion Sn, etc.).

2.3 Supporting Documents

- Agile accessible via the ValueChain website (<https://valuechain.dell.com/>) for Suppliers/Vendors.
- General Specification for Allowable Levels of Lead (Pb) in Dell Products (Dell P/N D4394) located in Agile.
- Lead Free Component Requirements (Dell P/N M4461) located in Agile.
- Dell Restricted Material Spec (Dell P/N 6T198) located in Agile.
- Dell Supplier Declaration on Restricted or Banned Materials (Dell P/N 7X435) located in Agile.
- Directive of the European Parliament and of the Council on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment, 2000/159/COD, October 2002. (RoHS Directive)
- Directive of the European Parliament and of the Council on Waste Electrical and Electronic Equipment, 2000/0158/COD, October 2002. (WEEE Directive)
- 91/157/EEC as amended by Directive 98/101/EC, Batteries and accumulators containing certain dangerous substances.

2.4 Procedure

Prior to the start of qualification testing it is expected that the supplier has performed extensive process optimization studies for Pb-free. DOEs should have been run to select the best solder paste material for screen printing and solder joint integrity. Optimum reflow parameters and an acceptable process window should be determined. Necessary wave solder and rework procedures

should be finalized and inspection methods determined. It is expected that the process conditions and materials used to build products for qualification are locked-in for the foreseeable future.

This qualification document consists of three levels of testing requirements. The qualification level is based on product complexity, reliability expectations and risk to customers. The Level 1 requirements apply to relatively simple Dell components/products with a lower implied risk of failure due to lead-free materials and processing. Level 2 applies to products with moderate complexity and risk of failure while Level 3 is meant to address more complex Dell products with highest expected reliability. Prior to initiation of testing, the supplier shall obtain written confirmation from Dell of the required qualification level required for their product.

Prior to any testing a detailed test plan should be developed and agreed upon by all involved parties. This plan should include specific tests, testing location, sample sizes, pass/fail criteria, etc. Sample sizes for component level testing and evaluation will be according to specification unless specifically modified by Dell. Reliability evaluation will be performed at a Dell approved test site unless otherwise agreed prior to start of the project.

A control group will be required for comparison purposes and may consist of the same product assembled with SnPb solder or a previous generation of SnPb product of same complexity. Control group type will be determined by mutual agreement between Dell and the supplier.

The qualification criteria listed are in addition to standard qualification testing already expected of the supplier and any used by the supplier to qualify their current processes. Each supplier is required to submit a report detailing the test conditions, sample sizes, evaluation procedures and test results for any testing that was performed separately from Dell requirement.

At Dell discretion, based on coverage of testing already performed and results provided, all or part of the requirements in this document may be modified. In some cases Dell may require additional testing to determine test limits and failure mechanisms associated with certain higher risk components.

3.0 Qualification Requirements for Level 1

This level is reserved for products with lower perceived risk of failure due to introduction of lead-free materials and processing. Products determined to be in this level are relatively simple and constructed exclusively with components such as passives, through-hole and/or coarse pitch (>0.5 mm) surface mount leaded packages. Some exceptions may apply based on specific product application or use environment. To ensure that all materials can survive the elevated temperatures expected with lead free assembly, all components must be evaluated individually prior to assembly. Types of failure mechanisms being screened for include heat damage, moisture induced cracking/delamination, poor solderability, and weak joints.

NOTE: The following information in sections 3.1, 3.2, and 3.3 must be provided to Dell in a timely fashion upon request.

3.1 Materials Used

- a) PCB type
- b) PCB Manufacturer
- c) PCBA Assembler (list if sub contracted, In House, sub supplier)
- d) PCB glass transition temperature
- e) PCB decomposition temperature
- f) PCB manufacturer certified heat resistance
- g) PCB Thickness
- h) PCB # Layers
- i) 1 or 2 side populated
- j) Pad finish type (i.e.ImAg, OSP, etc.)
- k) List the surface mount lead-free alloy (i.e. Sn-3.5Ag-0.9Cu)
- l) Solder paste manufacturer and product # (list all suppliers)
- m) SIR test results from solder paste supplier.
- n) Flux type (no clean, water soluble, etc.)
- o) Wave solder Pb-free alloy
- p) Hand Solder / Rework (Wire) Pb free alloy

3.2 Process Information

The information requested below is important to both supplier quality and reliability engineering in relation to lead free process and reliability impact. The questions are meant to establish a baseline for these items relative to initial lead free process management and will be evaluated by both SQE and Reliability. Ongoing processes and controls will be managed by the Supplier Quality organization.

1. Is the product built with a single or dual reflow process?
2. List the peak temperature distribution across the PCBA/Panel.
3. Time within +/-5C of peak.
4. List the time above liquidus temperature.
5. Provide time / temperature reflow profile. Provide location on PCB / Panel for thermocouple probes (attach picture / diagram) and temperatures for those locations during the reflow process.
6. List the minimum peak solder joint temp measured on board (under highest thermal mass component).
7. Wave solder process flow and maximum solder pot temperature / duration (if applicable).
8. Soldering iron temperature (Temp +/-) for rework and hand solder. Maximum allowable hand-solder duration.
9. Provide general overview of part storage and factory floor management for components according to MSL level (for moisture sensitive components). Detailed part management is subject to on site audit.
10. Is nitrogen used in reflow?
11. Procedures for rework to include inspection criteria and soldering iron temperature.
12. Inspection criteria used for lead-free solder joints. This will include criteria for sub contracted assemblies.
13. Provide general overview regarding isolation and tracking of leaded components / materials from Pb-free components / materials. Detailed part management is subject to on site audit.

3.3 Component Information

3.3.1 Heat Resistance

All components used to build a Pb-free product must be rated for temperatures at least 10°C higher than peak assembly process temperature. Heat resistance testing should be performed following MIL-STD 202G #210F with 90-120sec above Pb-free solder liquidus with ≥ 10 seconds at or above peak or equivalent. MIL-STD-202G #210F should be followed for wave solder and soldering iron heat resistance evaluation. Components should be rated for a soldering iron temperature of at least 10°C higher than process conditions.

3.3.2 Moisture Sensitivity

Determining the moisture level for surface mount components should be done following J-STD-020B (or latest release) for Pb-free or JEITA ED 4701 (Test Method 301A for Pb-Free). Sample sizes are defined in the specifications as well as inspection and pass/fail criteria. A minimum of Level 3 (JEDEC) or Level E (JEITA) is required for all components. Level 4 components (JEDEC) or Level F/G (JEITA) may be approved if factory management is considered acceptable by Dell. Components that do not meet minimum of Level 4 or above are not acceptable.

3.3.3 Lead Plating

The Pb-free lead plating material is important in evaluating the risk for tin whiskers. Table 1 outlines requirements for Tin Whisker testing for plating materials determined to be a risk. Finer pitch components plated with Sn based lead finish are most susceptible to shorting due to whisker growth. A 1.3 μm nickel underplate is preferred for Sn finishes as this prevents copper diffusion into the Sn which contributes to compressive stress in the Sn layer (the primary driving force for Sn whiskers). SnCu plating is known to be a high risk for Sn whisker growth and should be avoided when possible (bright Sn is the highest risk and not acceptable for use in Dell products without consent). Lead plating situations as outlined in table 1 will require testing according to NEMI/JEITA recommended procedures: 1) Storing at 60°C/95%RH for 1000 hours followed by SEM analysis; 2) Thermal cycling 1000 times from -55°C/85°C followed by SEM analysis; and 3) Store at room atmosphere conditions for 1000 hours followed by SEM. The maximum allowable whisker length is 50 microns.

Table 1. Tin Whisker Risk Matrix

Finish	Lead Pitch > 0.5mm	Lead Pitch $\leq 0.5\text{mm}$	Comments
Sn/Ni (>1.3 μm Ni)	Acceptable	Acceptable	Best Sn based option for connectors or flex circuits
SnBi (1-4%Bi)	Acceptable	Acceptable	Should not combine with SnPb solder due to reliability risk
SnAgCu & SnAg	Acceptable	Acceptable	Difficult to electroplate
Sn (matte)	Acceptable	Testing Required	Reflow or annealing may help reduce Sn whisker density (conflicting industry data).
SnCu	Acceptable	Testing Required	For high reliability applications testing may be required for >0.5mm pitch
Sn (bright)	Unacceptable	Unacceptable	Semi-bright Sn should be treated similar to SnCu

3.4 Sample Distribution

1. Full sample size must be provided from each manufacturing location *and solder supplier* used.
2. If different manufacturing lines used, then sampling must be from each line. Sampling rate will be determined by Dell and the supplier prior to evaluation.
3. Distribution of key components from each manufacturer used. Definition of key component includes both supplier of major component and lead free / non lead free components (including passives). Key component(s) and build mix will be determined by Dell and the supplier prior to evaluation.
4. A control group will be required for comparison purposes. This control group may consist of the same product assembled with SnPb solder or previous generation of SnPb product of same complexity. Control group type will be determined by mutual agreement between Dell and the supplier.

3.5 Assembly and Inspection (this step is not required for Level 2 and Level 3 products where 4.1 applies).

1. Assemble at least 10 boards with predetermined optimal assembly conditions.
2. Provide PCBA information in a spreadsheet:
 - a. Where assembled (location).
 - b. Name of PCBA assembler (if not in-house).
 - c. Function of PCB (i.e. main PCB, motor control, etc.).
3. Visually inspect all components on boards (with up to 40x magnification) for defects (cracking, delamination, etc.) and record all observations. Provide component inspection standards (i.e. pass/fail criteria) used for this inspection. **NOTE:** Dell reserves the right to specify inspection method if supplier inspection method is deemed insufficient.
4. Prove each component (passive and active) meets electrical performance specifications either individually or by functionally testing the entire board.
5. Visually inspect solder joints for defects (with up to 40x magnification). Inspection standard IPC-A-610 can be used for solder joint defects until a specific lead-free standard is released.
6. Visual inspection and functional test specifics should be agreed upon with Dell prior to commencement of test.
7. For key IC package components (determined by Dell and Supplier prior to test), perform C-SAM and X-ray after assembly (sample size ≥ 5) to evaluate component and solder joint integrity (i.e. level of voiding in joints).
8. Criteria: Component delamination must meet criteria according to J-STD-020B. Solder joint voiding shall be less than 25% of area. Zero electrical failures. No critical soldering defects.
9. Representative solder joints shall be cross-sectioned to ensure a properly reflowed solder joint (with 1-2 μm intermetallic layer thickness). Inspection and analysis results will be provided to Dell according to agreed upon timeline and reporting method.

An example of a level 1 test flow chart is shown in the Appendix.

Note: Additional evaluation may be required based on specific product application or use environment.

4.0 Qualification Requirements for Level 2

This level is reserved for products with moderate perceived risk of failure due to introduction of lead-free materials and processing. Products determined to be in this level are more complex and will likely have one or more of the following surface mounted components: plastic leadless packages, fine pitch QFPs (≤ 0.5 mm lead pitch), plastic ball grid arrays (≤ 27 mm body size) or chip scale packages with ball pitches ≥ 1 mm (ball pitch of less than 1mm is reserved for Level 3). In addition to the Level 1 requirements of proving process capability and functionality after assembly, this level of qualification requires testing for mechanical and thermally induced fatigue failure. This Level requires that the product also pass qualification Level 1.

4.1 Precondition / Assembly

Assembly of product/test boards should be done at optimum process conditions (including wave or hand solder when applicable) followed by reworking of predetermined components on some boards. In some cases exploring additional assembly conditions may be required. For example, preconditioning components and boards prior to assembly is an effective way to prove that worst-case assembly conditions still produce reliable products (i.e. a sufficiently wide process window exists). A test plan specific to each product will be developed and sample sizes for each assembly condition agreed to prior to testing.

1. Minimum sample sizes for each condition are outlined in Table 2 for prime and rework.
2. Assemble components onto boards through the optimum lead free soldering process.
3. Perform rework of selected components.
4. Prove each component (passive and active) meets electrical performance specifications either individually or by functionally testing the entire board.
5. In cases where predetermined IC packages are selected for preconditioning, follow JEDEC Standard 22-A113D and expose to level 3 moisture conditions. Preconditioning boards prior to assembly should take place per J-STD-003A (8 hr steam age for Sn plated finish, 35C/85% for 24 hours for OSP finish, and 85°C/85%RH for 12 hours for immersion Ag).
6. Perform C-SAM and X-ray on key IC package components after assembly and rework if required (determined by Dell and Supplier prior to test). Minimum sample sizes are shown in Table 2.
7. Visually inspect (with up to 40x magnification) all components on boards for defects (cracking, delamination, etc.) and record all observations. Provide component inspection standards (i.e. pass/fail criteria) used for this inspection. **NOTE:** Dell reserves the right to specify inspection method if supplier inspection method is deemed insufficient.
8. Visually inspect (with up to 40x magnification) solder joints for defects. Inspection standard IPC-A-610 can be used as inspection standard for solder joint defects until standard is released for lead-free.
9. To establish a baseline prior to reliability testing, major components on one PCBA should be cross sectioned after assembly while those on another PCBA should be subjected to Die & Pry.
10. Criteria: Component delamination from C-SAM must meet criteria according to J-STD-020B. Zero electrical failures are allowed. No critical soldering defects (voiding should be less than 25% of joint area as revealed in X-ray inspection).
11. Use these assembled boards for reliability tests according to test plan.
12. Test and failure analysis results will be provided to Dell according to agreed upon timeline and reporting method.

4.2 Vibration and Shock

Concurrent testing for both vibration and shock shall be performed when determined to be necessary by the Dell Shock and Vibration Group. Testing details will be prescribed according to the product type and expected use environment. Typical tests may include non-operational vibration followed by shipping shock (pack drop). In some instances mechanical shock and vibration testing may be preceded by thermal shock. Operational testing in a system level may also be performed. Sample sizes and pass/fail criteria will be determined during creation of the detailed test plan (sample size will typically be 5 or greater for each test type).

4.3 Thermal Cycling

This testing is required primarily for level 2 components. These devices should be agreed upon with Dell prior to testing. Follow procedures described in JESD22-A104-B, condition J. The specific requirements described below fit many product types, however, alternative thermal cycling test protocols and evaluation plans are potentially acceptable if approved by the Dell Reliability Engineer.

1. Sample sizes shown in Table 2.
2. The complete functional PCBA must be thermal cycle tested.
3. Cycle 1000 times from 0 to 100°C with a ramp rate of 10-20°C/min and a 10 min dwell time (measure temperature on the largest thermal mass component on the PCB).
4. Visually inspect joints and confirm functionality of complete PCBAs after 500 and 1000 cycles.
5. In cases where proving electrical functionality is not feasible, solder joints on BGA components can be evaluated after 1000 cycles using dye and pry.
6. Criteria: Zero solderjoint failures accepted unless product life requirements allow for a failure.
 - a. A failure is defined by a functional test error or a joint that is cracked 100% through (as revealed by dye and pry).
 - b. Visual inspection and functional test specifics to be agreed upon with Dell prior to commencement of test. Additional inspection may include cross sectioning, lead pull, and component shear.
7. Test and failure analysis results will be provided to Dell according to agreed upon timeline and reporting method. Solder joint failures will be assessed and corrective actions taken.

4.4 Highly Accelerated Life Testing (HALT)

NOTE: HALT procedures are not currently established on all products at Dell. Where procedures are not defined, Dell will work closely with each supplier to evaluate the feasibility of implementing PCBA level HALT test and the setup and implementation of that process. Listed below are minimum acceptable test conditions according to current practice.

1. HALT is primarily a board level test that must be performed at a Dell approved facility and according to current Dell procedures (occasionally HALT may be used on a system level).
2. During the HALT process, thermal cycling and vibration are to be simultaneously applied.
3. Consult with Dell reliability engineering for the test method dependent on specific product involved. Dell must agree in writing to procedures used for evaluation.

4. The temperature responses on critical components must be monitored with thermocouples to insure adequacy of the dwell periods selected
5. The temperature range (between highest and lowest dwell temperatures) is to be a minimum of 80-degrees C unless otherwise agreed by Dell reliability.
6. The product is to be functionally operational and monitored during "HALT" stressing unless otherwise agreed to Dell reliability.
7. Sample size is shown in Table 2.
8. Where a previously established baseline is available, the product must meet or exceed prior limits. Where no prior baseline is established, comparative results to leaded control sample must be met.
9. Dell Reliability Engineering must agree to test and evaluation methodology prior to commencement of HALT testing.
10. Supplier is to report test results according to agreed upon format, including full failure analysis and corrective action on anomalies observed
11. Criteria: Component delamination must meet criteria according to J-STD-020B. Zero functional failures, or fully cracked solder joints.

An example of a level 2 test flow chart is shown in the Appendix.

5.0 Qualification Requirements for Level 3

This level is reserved for products with higher perceived risk of failure due to introduction of lead-free materials and processing. Products determined to be in this level are highly complex and will likely have less proven surface mounted components such as large and fine pitch BGAs, ceramic BGAs or leadless packages, chip scale packages with < 1 mm ball pitch, flip chip devices, BGAs with mounted heat spreaders, and/or packages made with microvia circuit boards. Products tested to this level may also include those where the use environment is harsh and/or failure is more costly to the customer (i.e. causing data loss or critical down time). This qualification level requires that the product also pass the tests outlined in Qualification Level 1 and Level 2.

5.1 Thermal Cycling to Failure

1. Sample size: ≥ 30 . A separate group of an additional 10 reworked components will also require testing to failure. This testing is typically performed on specific high risk components using daisy chain patterns to evaluate second level solder joints. Testing to failure enables Dell to estimate the life of these components under typical use conditions. For components that are non-daisy chained, discuss testing details with Dell prior to execution of test.
2. Procedure:
 - a. Cycle to $\geq 60\%$ cumulative device failure (-40°C to 125°C) per JESD22-A104-B condition G. Risk assessment will be made after 2000 cycles to determine continuation of test. Note: lower thermal cycle temperature ranges are acceptable, however additional time will be required to achieve $\geq 60\%$ failure.
 - b. A minimum of a 10 minute dwell is required at each temperature (longer dwell times preferred).
 - c. Temperature change rate of $10\text{-}20^{\circ}\text{C}$ / minute as measured on the largest thermal mass component on the PCB.
 - d. Continuous monitoring preferred, but room temperature, in-circuit probe testing at 200 cycle intervals is acceptable.
 - e. Plot 2 parameter Weibull distribution to obtain α and β values.
3. For daisy chained component an electrical failure is defined as a delta R of $> 300\text{ohms}$ or a 50% increase, (or a value agreed upon with Dell Corporation).
4. Provide Weibull plot and associated variables (α , β).
5. Test and failure analysis results will be provided to Dell according to agreed upon timeline and reporting method.

5.2 Torsion Testing (for notebook computers only)

Boards assembled for laptop computers will require torsion testing to ensure the ability to survive expected twisting or bending which occurs in the use environment. This testing may be done at the PCBA level or system level or both.

1. A minimum of 5 samples should be tested.
2. Apply system flex/twisting forces according to Dell Test Procedure REL0019.
3. Visually inspect and functionally inspect according to specification.

- Criteria: Zero failures due to Pb-free solder materials or the elevated processing temperatures (failures due to other causes should be addressed separately).

5.3 BGA Package Coplanarity

- This test should be applied to molded BGA packages with an edge length of 31mm or greater. This test is required to ensure that unacceptable warping of the package does not occur at Pb-free reflow temperature thus providing the potential for poorly formed or open solder joints at the corners of the array.
- Sample size: >3 components (it is expected that this test be performed by the component supplier).
- Follow JESD22-B108A at 220°C to confirm that the coplanarity of the package substrate falls within an 8 mil specification at reflow temperature (note: this is not a solderball coplanarity measurement but a measurement of the package body). Shadow Moire' analysis is recommended for this test.

An example of a level 3 test flow chart is shown in the Appendix.

Table 2. Pb-Free Qualification Summary

Assembly/Test Requirements	Level 1 (desired sample sizes)	Level 2 (desired sample sizes)	Level 3 (desired sample sizes)
Provide requested material information			
Provide requested process information			
Provide certified component heat resistance			
Provide component moisture sensitivity levels	≥ 11 components	≥ 11 components	≥ 11 components
Provide component lead finish and whisker test results where necessary			
Assemble and inspect boards (C-SAM, X-ray, x-section, and functionally test).	≥ 10 boards		
Assemble PCBAs at optimum conditions and rework selected major components (include SnPb control group when possible).		≥ 30 prime ≥ 18 rework	≥ 55 prime ≥ 28 rework
Functional verification (or electrical continuity test)		100%	100%
Visual inspection		100%	100%
C-SAM major components		≥ 5 prime ≥ 3 rework	≥ 5 prime ≥ 3 rework
X-ray selected BGA components		≥ 5 prime ≥ 3 rework	≥ 5 prime ≥ 3 rework
Cross-section selected components		≥ 2 prime ≥ 2 rework	≥ 2 prime ≥ 2 rework
Thermal cycle PCBA 0/100C, 1000 cycles.		≥ 20 prime ≥ 10 reworked	≥ 20 prime ≥ 10 reworked
HALT		≥ 4 prime ≥ 3 rework	≥ 4 prime ≥ 3 rework
Vibration and Shock (concurrent). Details to be provided by Dell Shock and Vibration Group.		≥ 4 prime ≥ 3 rework	≥ 4 prime ≥ 3 rework
Thermal cycle selected components (-40/125C or other range) to at least 60% cumulative failures (typically performed with daisy chain components).			≥ 20 prime ≥ 10 rework
Torsion test laptop (PCBAs and/or system)			≥ 5
Warpage measurement of large PBGA packages (≥ 31mm)			≥ 3

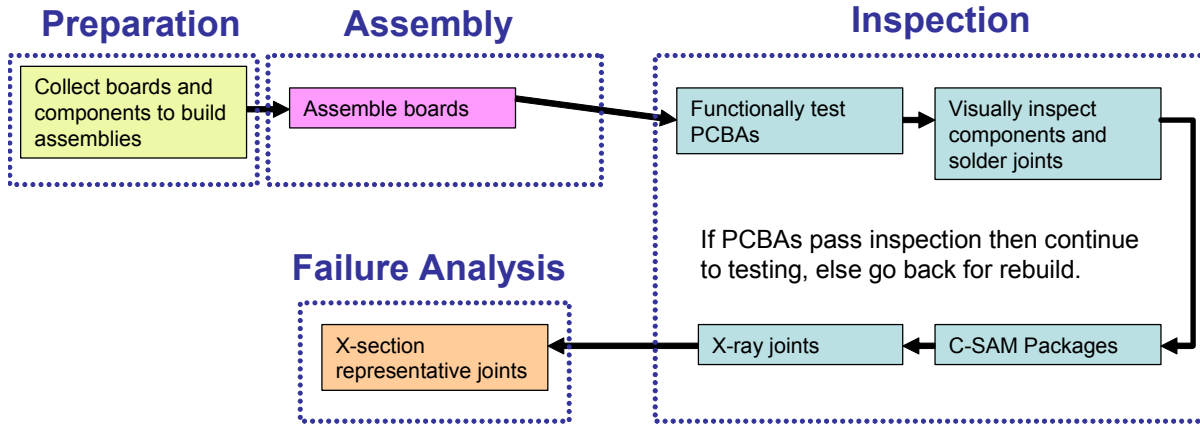
6.0 Appendix: Pb-Free Risks

SnPb solder materials have been used in the electronics industry for over 60 years and therefore the processing conditions and their impact on materials and reliability are well understood. Converting to Pb-free materials and processes introduces many risks some of which are better understood than others. The following table describes some of the changes inherent with Pb-free, the failure mechanisms they may induce and the testing/inspection procedures used to screen for them. The test criteria called out in this Pb-free qualification document are intended to screen for many of these potential failure mechanisms.

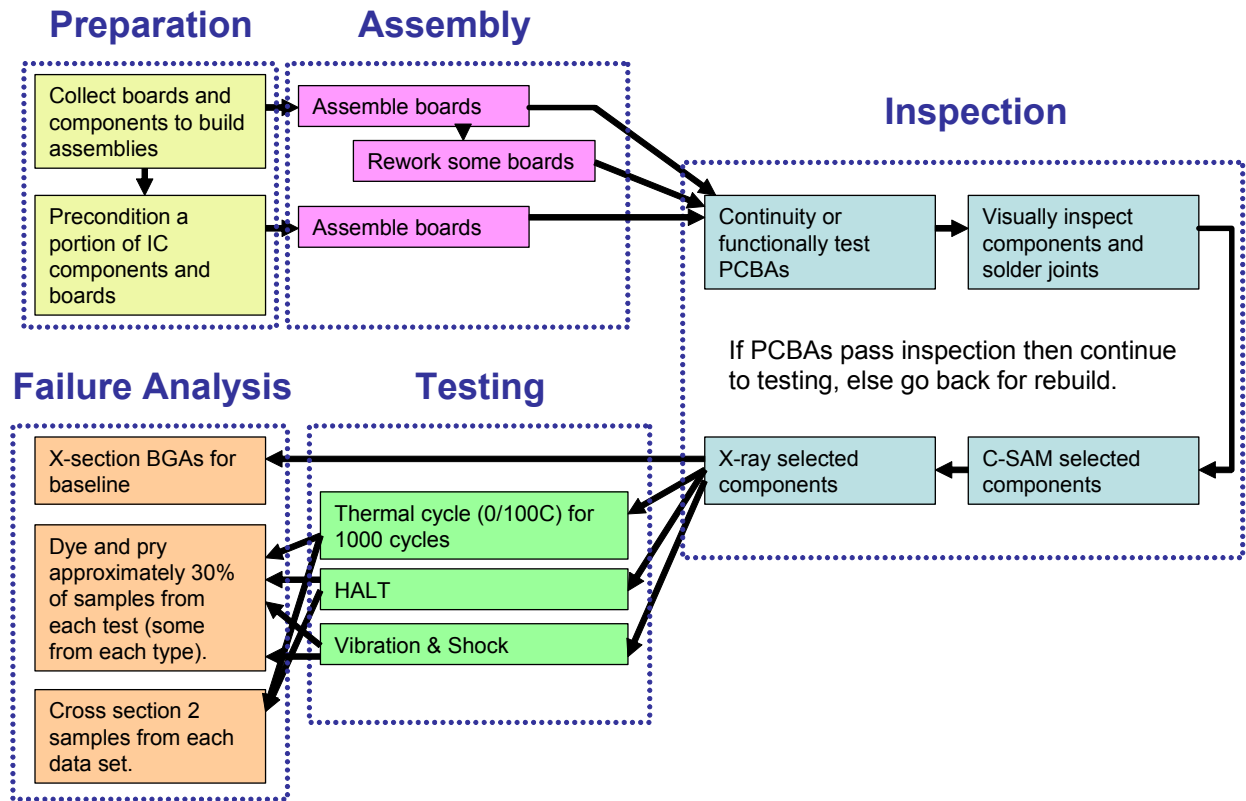
Area of Concern	Impacted Item	Failure Mechanism	Testing Method	Inspection Technique
Moisture sensitivity	Plastic IC packages, optocouplers, other polymer based components	Popcorn delamination at higher reflow temperatures. Heat damage of IC packages	Moisture sensitivity testing. J-STD-020B	Visual inspection C-SAM
Heat damage	All passive components, circuit boards	Cracking, dielectric breakdown (capacitors), PCB delamination, warping, or via cracking	Heat resistance MIL-STD 202G #210F Decomposition temp. Time to delamination Package planarity JESD22-B108A fee required	Visual inspection, functional verification
Poor wetting	All solder joints	Cold joints or weak joints fracture in use environment	Solderability J-STD-002B J-STD-003A	Wetting balance, visual inspection, x-sectioning, lead pull
Solder fatigue	Solder joints, particularly on high CTE components	Cracked solder joints	Thermal cycle JESD22-A104-B , HALT Vibration	Electrical continuity Visual inspection
Mechanical shock	Solder joints particularly on higher mass components	Solder joint failure during shipping or dropping	Shock test	Electrical continuity Visual inspection
Sn whiskers	Sn and SnCu plated components	Shorting	NEMI / JEITA recommended procedures	SEM
Surface mount process control	Insufficient process window creates poor solder joints	Occasional solder joint failures in use environment	Precondition and assembly JEDEC Standard 22-A113D fee:\$45	X-ray, X-section, Inspection, reliability test
Rework process	Poor solder joints, damaged components,	Joint failures or cracked vias in use environment	Rework components followed by reliability testing	X-ray, X-section, Inspection, reliability test
Wave solder process	Incomplete hole fill, fillet lifting, damage to board	Failed through hole, cracked vias, weak joints	Thermal cycle HALT Vibration	Electrical continuity, visual inspection
Electrochemical migration	Board surface with no-clean paste residue	Shorting between biased traces in a moist environment	Bellcore GR-78-CORE J-STD-004 SIR	Visual and resistance after 35C/85%RH exposure at 50V

6.1 Appendix: Examples of Test Flows

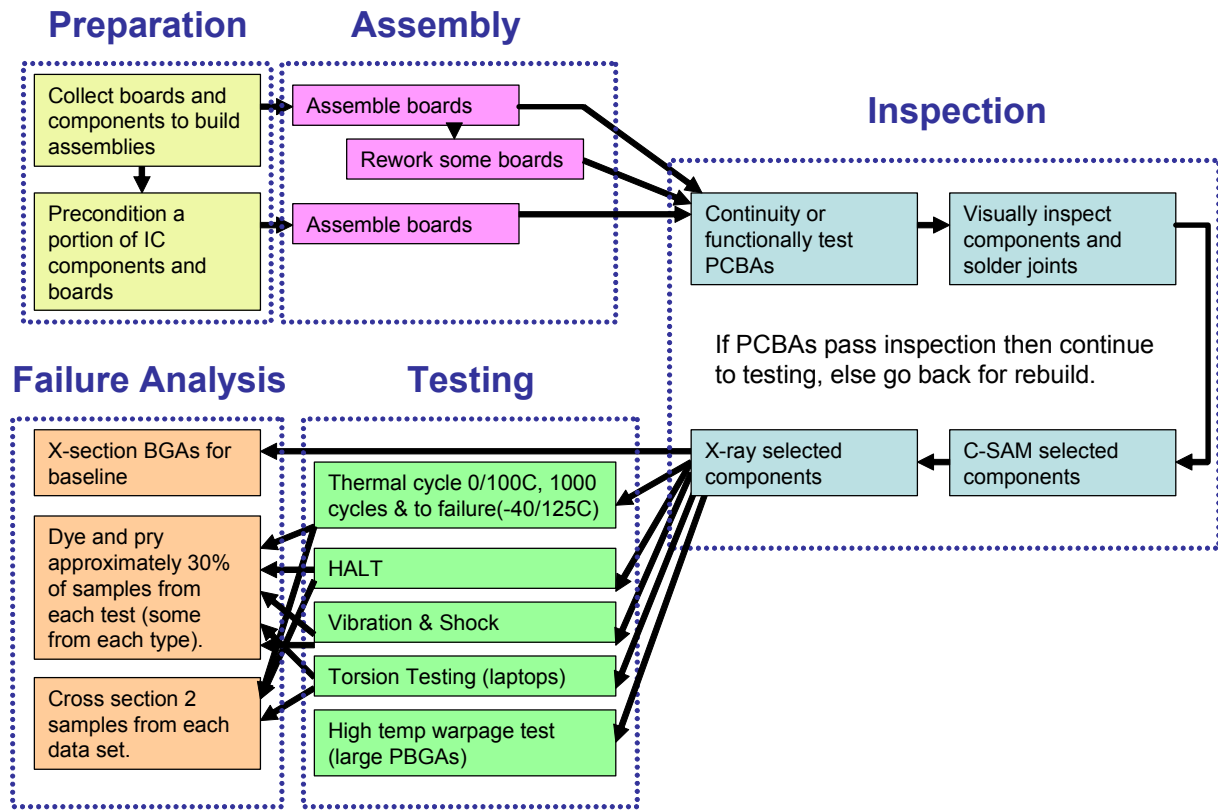
Pb-Free Reliability Test Flow – Level 1



Pb-Free Reliability Test Flow – Level 2



Pb-Free Reliability Test Flow – Level 3



7.0 References

1. Mil-STD-202G, Method 210F “Resistance to Soldering Heat”, February 2002. Must meet modified test conditions according to Dell requirement and Lead Free solder used.
2. J-STD-020B “Moisture / Reflow Sensitivity Classification for NonHermitic Solid State Surface Mount Devices”, July 2002 (020C to be released soon).
3. J-STD-002B “Solderability Tests for Component leads, Terminations, Lugs, Terminals, and Wires”, February 2003.
4. J-STD-003A, “Solderability Tests for printed Circuit boards”, February 2003
5. JESD22-A113-D, “Preconditioning of Nonhermetic Surface Mount Devices Prior to”,
6. IPC-A-610C, “Acceptability of Electronic Assemblies”, January 2000
7. Dell internal HALT standard, contact Dell for specifics.
8. IPC-9701 “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachment”, January 2002
9. MIL-STD-883E, method 2022.2, “Wetting Balance Solderability”, 1996.
10. IPC-SM-785 “Guidelines for Accelerated reliability Testing of Surface Mount Solder Attachments.”, November 1992
11. MIL-STD-202G, Method 208H, “Solderability”, February 2002
12. JESD22-B108-A “Coplanarity Test for Surface-Mount Semiconductor Devices”, Jan., 2003.
13. JESD22-A104-B “Temperature Cycling”, July, 2000.
14. JESD22-B103-B “Vibration, Variable Frequency”, June, 2002.
15. JESD22-B104-B “Mechanical Shock”, March, 2001.